Intel® High Definition Audio Specification
Document Change Notification

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Change Identification: **DCN No: HDA016-A**
Document Revision: Intel® High Definition Audio 1.0

Title: Clarification for Read Only (RO) register bits

Brief description of the functional changes proposed:

During test development at Microsoft it was attempted to write to read only fields and then check to see if there were are "hidden" bits or anomalous behavior. Such behavior was seen in some controllers. This ECR is to clarify that writing to Read Only bits may produce undetermined behavior and is prohibited.

Current Definition:

3.1.2 General Register Behaviors and Access Requirements

All controller registers must be addressable as byte, Word, and Dword quantities. The software must always make register accesses on natural boundaries; Dword accesses must be on Dword boundaries; Word accesses must be on Word boundaries; etc.

Software must also properly handle reserved bits. Reserved bits may be designated "RsvdP" or "RsvdZ." Bits marked "RsvdP" must be preserved using read-modify-writes, while "RsvdZ" bits must be written as 0's. This handling helps to ensure future compatibility.

Note that host controllers are not required to support exclusive-access mechanisms (such as PCI LOCK) for accesses to the memory-mapped register space. Therefore, if software attempts exclusive-access mechanisms to the host controller memory-mapped register space, the results are undefined.

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3.3.42 Offset 98h: {IOB}SDnBDPL – Input/Output/Bidirectional Stream Descriptor *n* BDL Pointer Lower Base Address

Length: 4 bytes

Table 1. Stream Descriptor *n* Lower Base Address

Bit	Type	Reset	Description
31:7	RW	0's	**Buffer Descriptor List Lower Base Address (BDLLBASE):** Lower address of the Buffer Descriptor List. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. This value should not be modified except when the RUN bit is 0.
6:0	RO	0's	Hardwired to 0 to force 128-byte alignment of the BDL.

New Definition:

3.1.2 General Register Behaviors and Access Requirements

All controller registers must be addressable as byte, Word, and Dword quantities. The software must always make register accesses on natural boundaries; Dword accesses must be on Dword boundaries; Word accesses must be on Word boundaries; etc.

Software must also properly handle reserved bits. Reserved bits may be designated "RsvdP" or "RsvdZ." Bits marked "RsvdP" must be preserved using read-modify-writes, while "RsvdZ" bits must be written as 0's. This handling helps to ensure future compatibility.

Fields or Registers marked as Read Only (RO) when part of a Register that is Read/Write may be written, but the RO bits must contain the exact bit values that are returned when reading the register, e.g. treated as RsvdP. Writing values that do not match values read from a RO field into that RO field may cause indeterminate behavior.

Note that host controllers are not required to support exclusive-access mechanisms (such as PCI LOCK) for accesses to the memory-mapped register space. Therefore, if software attempts exclusive-access mechanisms to the host controller memory-mapped register space, the results are undefined.

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6:0	RsvdZ	0's	Hardwired to 0 to force 128-byte alignment of the BDL. Attempting to write any value other than zero to this field may result in unspecified behavior.